DESCRIPTION

SEMICONDUCTOR LIGHT EMITTING ELEMENT, MANUFACTURING METHOD THEREOF, INTEGRATED SEMICONDUCTOR LIGHT EMITTING DEVICE, MANUFACTURING METHOD THEREOF, IMAGE DISPLAY DEVICE, MANUFACTURING METHOD THEREOF, ILLUMINATING DEVICE AND MANUFACTURING METHOD THEREOF

Technical Field

This invention relates to a semiconductor light emitting element, manufacturing thereof, integrated semiconductor light emitting device, manufacturing method thereof, image display device, manufacturing method thereof, illuminating device and manufacturing method thereof, which are especially suitable for application to light emitting diodes using nitride III-V compound semiconductors.

Background Art

The Applicant already proposed a light emitting diode as a semiconductor light emitting element. This semiconductor light emitting element was made by growing an n-type GaN layer on a sapphire substrate; next forming thereon a growth mask having a predetermined opening; selectively growing an n-type GaN layer in form of a six-sided pyramid having an inclined crystal plane inclined from the major surface of the substrate, i.e. having an S-oriented plane; and

growing an active layer, p-type GaN layer and other layers on the inclined crystal plane (see, for example, brochure of International Publication No. 02/07231 (pages 47-50 and Figs. 3-9)). This light emitting diode can prevent propagation of penetrating dislocations from the substrate side to layers composing the element structure, and can improve the crystalline property of these layers, high emission efficiency can be obtained.

Figs. 1A and 1B show a typical semiconductor light emitting element disclosed in the above-mentioned literature. This semiconductor light emitting element is manufactured by the following method. An n-type GaN layer 102 is first grown on a sapphire substrate 101 having a C+ oriented major surface. After that, a SiO_2 film is formed on the entire surface of the n-type GaN layer 102, and it is patterned by lithography and etching to make a growth mask 104 having an opening of a predetermined geometry in a position for forming the element. The geometry of the opening 103 is a circle or a hexagon having one side parallel to the <11-20> direction. Size of the opening 103 is about 10 μm. In the next step, under the existence of the growth mask 104, an n-type GaN layer 105 is selectively grown on a part of the n-type GaN layer 102 exposed through the opening 103. As a result of the selective growth, the n-type GaN layer 105 in form of a six-sided pyramid.

Six planes of the six-sided pyramidal n-type GaN layer 106 are S-oriented planes inclined from the major surface of the sapphire substrate 101. After that, an active layer 106 composed of InGaN compounds, for example, and a p-type GaN layer 107 are sequentially grown on the n-type GaN layer 105. Through these steps, here is obtained a double-hetero-structured light emitting diode structure including the six-sided pyramidal n-type GaN layer 105, active layer 106 and p-type GaN layer 107, the last two being grown sequentially on the inclined crystal planes of the six-sided pyramidal n-type GaN layer 105. In the next step, which is not explained here in detail, a p-side electrode is formed on the p-type GaN layer 107 and an n-side electrode is formed on the n-type GaN layer.

Existing semiconductor light emitting elements, having a light emitting element structure made by selectively growing the six-sided pyramidal n-type GaN layer 105 having an S-oriented inclined crystalline plane and next growing the active layer 106 and the p-type GaN layer 107 on the S-oriented plane, were unsatisfactory in light emitting efficiency, and inevitably required a large occupied area per each element.

It is therefore an object of the invention to provide a semiconductor light emitting element sufficiently high in light emitting efficiency and

small in occupied area per each element, as well as a manufacturing method of the semiconductor light emitting element.

Another object of the invention is to provide an integrated semiconductor light emitting device sufficiently high in light emitting efficiency and small in occupied area per each element, a manufacturing method thereof, an image display device, a manufacturing method thereof, an illuminating device and a manufacturing method thereof.

Disclosure of Invention

To accomplish the objects, the first aspect of the invention is a semiconductor light emitting element comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

Materials of the semiconductor layer of the first conduction type, active layer and semiconductor layer of the second conduction type are not limitative essentially. However, materials having a wurtzite crystalline structure are typically used. Examples of semiconductors having a wurtzite crystalline structure are nitride III-V compound semiconductors. In addition, II-VI compound semiconductors such as BeMgZnCdS compound semiconductors and BeMgZnCdO compound semiconductors can be given as such examples. Most widely, nitride III-V compound semiconductors are composed of $Al_xB_yGa_{1-x-y-z}In_zAs_uN_{1-u-v}P_v$ (where $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$, $0 \leq u \leq 1$, $0 \leq v \leq 1$, $0 \leq x+y+1 < 1$ and $0 \leq u+v < 1$). More specific examples are composed of $Al_xB_yGa_{1-x-y-z}In_zN$ (where $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$ and $0 \leq x+y+1 < 1$). Typical examples are composed of $Al_xGa_{1-x-z}In_zN$ (where $0 \leq x \leq 1$ and $0 \leq z \leq 1$). Concrete examples of nitride III-V compound semiconductors include GaN, InN, AlN, AlGaN, InGaN, AlGaInN, and so forth.

In case the semiconductor layer of the first conduction type has a wurtzite crystalline structure, the plurality of crystal planes as constituents of the inclined crystal plane of the convex crystal portion of

the semiconductor layer are typically S-oriented planes (including planes that can be regarded S-oriented planes substantially). Angles of inclination of the crystal planes as constituents of the inclined crystal planes become smaller from the bottom of the crystal portion toward the apex. This crystal portion typically has a steeple-shaped configuration, which is six-sided most typically. In this case, angles of inclination of the uppermost crystal planes of the crystal portion, i.e. the upper parts of the crystal planes involving the apex of the crystal portion, which compose the inclined crystal planes, are preferably in the range from 3 μm to 20 μm, or typically in the range from 10 μm to 15 μm.

The second aspect of the invention is a method of manufacturing a semiconductor light emitting element having: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second

electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

In the second aspect of the invention, the entirety of the first semiconductor layer of the first conduction type and the second semiconductor layer of the first conduction type corresponds to the semiconductor layer of the first conduction type.

Basically, any material may be used as the substrate provided it assures a good crystallographic property when the first semiconductor layer of the first conduction type, second semiconductor layer of the first conduction type, active layer, semiconductor

layer of the second conduction type, and so forth, are grown thereon. More specifically, here is usable a substrate made of sapphire (Al_2O_3) (including C-oriented plane, A-oriented plane and R-oriented plane), SiC (including 6H, 4H and 3C), nitride III-V compound semiconductors (such as GaN, InAlGaN, AlN, and the like), Si, ZnS, ZnO, LiMgO, GaAs, $MgAl_2O_4$ or the like. Preferably, a hexagonal crystalline substrate or a cubic crystalline substrate of one of those materials is used, but a hexagonal crystalline substrate is more preferable. In case the first semiconductor layer of the first conduction type, second semiconductor layer of the first conduction type, active layer and semiconductor layer of the second conduction type are made of nitride III-V compound semiconductors, a sapphire substrate having a C-oriented plane as its major surface may be used. The "C-oriented plane" herein involves any crystalline plane that slightly inclines therefrom up to about 5 to 6° and can be regarded as the C-oriented plane substantially.

For growth of the first semiconductor layer of the first conduction type, second semiconductor layer of the first conduction type, active layer and semiconductor layer of the second conduction type, metal organic chemical vapor deposition (MOCVD), hydride vapor phase epitaxy or halide vapor phase epitaxy (HVPE), for example, may be used. To ensure

that the inclined crystal plane of the convex crystal portion makes a good convex plane composed of a plurality of crystal planes different in angle of inclination, growth temperature for selective growth of the second semiconductor layer of the first conduction type among those layers is controlled preferably within the range from 920°C to 960°C, more preferably within the range from 920°C to 950°C, or still more preferably around 940°C. Growth rate for the selective growth is controlled preferably at or above 6 μm/h, or more preferably in the range from 6 μm/h to 18 μm/h. For growth of the active layer and the semiconductor layer of the second conduction type, growth temperatures are typically controlled lower by 20 to 40°C or more, for example, than the growth temperature of the second semiconductor layer of the first conduction type.

Basically, the growth mask may be made of any material provided nucleation on the growth mask is amply less than nucleation on the first semiconductor layer (in other words, growth on the growth mask is prevented), and selective growth is therefore assured. Typically, however, a silicon oxide nitride (SiON) film, silicon nitride (SiN (especially Si_3N_4) film or their lamination is used as the growth mask. Otherwise, the growth mask may be an aluminum oxide (Al_2O_3) film, tungsten (W) film and a laminated film combining any of these films and any of the above-

mentioned films. To assure that the second semiconductor layer becomes a good steeple-shaped or pyramidal configuration, especially six-sided, the growth mask is preferably a mask at least with its top surface being made of silicon nitride, such as a mask made of a silicon nitride film or a mask made by stacking a silicon nitride film on a silicon oxide film.

The opening of the growth mask may have any geometry. Typically, however, it is hexagonal or circular. In case the opening of the growth mask is hexagonal, at lest one side of the hexagon is preferably normal to the <1-100> direction or <11-20> direction to prevent that the semiconductor layer grown by using the growth mask deviates from the hexagon.

Size of the opening in the growth mask (maximum measure in the direction parallel to the major surface of the substrate) is preferably small to reduce the area occupied by the element. However, if it is excessively small, it tends to invite crystal defects such as dislocations, depositional defects or the like during selective growth of the second semiconductor layer. Taking these factors into consideration, size of the opening in the growth is roughly in the range from 1/4 to 1 time the size of the semiconductor light emitting element. For example, it is in the range from 2 μm to 13 μm. If a slightly smaller size is

preferable, the size of the opening is typically in the range from 2 μm to 5 μm or more preferably in the range from 2.5 μm to 3.5 μm. If a slightly larger size is preferable, the size of the opening is typically in the range 7 μm to 13 μm or more preferably in the range from 9 μm to 11 μm.

Typically, the second semiconductor layer is selectively grown to spread horizontally wider than the opening of the growth mask. However, this is not an indispensable requirement, but the second semiconductor layer may be grown within the limit of the opening.

Typically, the second semiconductor layer is selectively grown so that a steeple-like configuration is formed. However, after the second semiconductor layer is selectively grown such that a crystal plane substantially parallel to the substrate is formed on its top portion, an undoped semiconductor layer may be grown on the top portion. Thereby, in case the second electrode is formed on the semiconductor layer of the second conduction type whereas the first electrode is formed on the semiconductor layer of the first conduction type comprising the first semiconductor layer and the second semiconductor layer and a current is supplied between the first electrode and the second electrode, the undoped semiconductor layer grown to form the apex portion of the steeple-shaped crystal portion functions as a current blocking portion to

prevent the current from flowing thereto. Since the crystalline quality of the apex portion of the crystal portion is usually inferior to the other portion, this structure enables the current to flow bypassing the apex portion of the crystal portion assures that the current flows only through the other portion having a good crystalline quality, and contributes to enhancing the emission efficiency.

The growth mask is usually left also after completion of the selective growth. However, it may be removed after the selective growth. In this case, a step of removing the growth mask intervenes between the step of selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer in the opening of the growth mask and the step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

In addition to the above-mentioned matters, the matters explained in conjunction with the first aspect of the invention are applicable to the second aspect of the invention as far as they are consistent with its nature.

The third aspect of the invention is an integrated semiconductor light emitting device including a plurality of integrated semiconductor light

emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

To assure that the inclined crystal plane of each convex crystal portion exhibits a good convex plane composed of a plurality of crystal planes different in angle of inclination, size of each opening of the growth mask is preferably in the range from 1/4 to 1 time the size of each semiconductor light emitting element, in general. More specifically, it is in the range from 2 μm to 13 μm. If a slightly smaller size is desirable, it is typically in the range from 2 μm to 5 μm, or preferably in the range from 2.5 μm o 3.5 μm.

If a slightly larger size is desirable, it is typically in the range from 7 μm to 13 μm, or preferably in the range from 9 μm to 11 μm. Distance between openings of the growth mask is generally a double or more of the size of each semiconductor light emitting element. More specifically, it is 10 μm or more, preferably 13 μm or more, or typically in the range from 13 μm to 30 μm.

The integrated semiconductor light emitting device can be used for any purpose. Its typical applications will be image display devices and illuminating devices, for example. The integrated semiconductor light emitting device contemplates both a device including a plurality of semiconductor light emitting elements monolithically formed on a common substrate and a device including a plurality of semiconductor light emitting elements that are first monolithically formed on a common substrate, then divided to discrete elements and then mounted on another substrate.

The fourth aspect of the invention is a method of manufacturing an integrated semiconductor light emitting device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a

plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

The fifth aspect of the invention is an image display device including a plurality of semiconductor

light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

The sixth aspect of the invention is a method of manufacturing an image display device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction

type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

The seventh aspect of the invention is an illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a

convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

The eighth aspect of the invention is a method of manufacturing an illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each including: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first

electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

In the third to eighth aspects of the invention, the matters explained in conjunction with the first and second aspects of the invention are applicable as far as they are consistent with their natures.

The ninth aspect of the invention is a semiconductor light emitting element comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a

convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

The tenth aspect of the invention is a method of manufacturing a semiconductor light emitting element having: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

The eleventh aspect of the invention is an integrated semiconductor light emitting device including a plurality of integrated semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

The twelfth aspect of the invention is a method of manufacturing an integrated semiconductor light emitting device including a plurality of integrated semiconductor light emitting elements each having: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second

semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

The thirteenth aspect of the invention is an image display device including a plurality of semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

The fourteenth aspect of the invention is a method of manufacturing an image display device integrating a plurality of integrated light emitting

elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

The fifteenth aspect of the invention is an illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

The sixteenth aspect of the invention is a method of manufacturing an illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each including: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a

second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

In the ninth to sixteenth aspects of the invention, each inclined crystal plane forming a substantially convex plane as a whole may locally include a flat plane.

In the ninth to sixteenth aspects of the invention, the matters explained in conjunction with

the first and second inventions are applicable as far as they are consistent with their natures.

According to the invention having the above-summarized configuration, the semiconductor layer of the first conduction type is selectively grown under the existence of the growth mask having the opening in a predetermined portion. Thereby, it is possible to make a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes different in angle of inclination to exhibit a good convex plane as a whole or having an inclined crystal exhibiting a substantially convex plane as a whole. Then, by sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the crystal plane, the light emitting element structure can be formed. In this case, the semiconductor layer of the second conduction type also has an inclined crystal plane composed of a plurality of crystal planes different in angle of inclination to exhibit a good convex plane as a whole, or an inclined crystal plane exhibiting a substantially convex plane as a whole. Therefore, in operation of the element, light generated from the active layer can be extracted efficiently by reflection at the inclined crystal plane of the semiconductor layer of the second conduction type, which exhibits the convex plane or the substantially convex plane. Moreover, in comparison

with a structure in which the crystal portion has an S-oriented inclined crystal plane, the present invention can diminish the size of the crystal portion and can therefore reduce the size of the light emitting element structure made by sequentially growing the active layer and the semiconductor layer of the second conduction type on the crystal portion. Furthermore, since the light extracting direction can be closer to the direction normal to the major plane, light is less subjected to blockage even when a black mask, or the like, is placed in the portion other than the light emitting portion.

Brief Description of Drawings

Figs. 1A and 1B are a plan view and a cross-sectional view of a conventional GaN-based light emitting diode;

Figs. 2A and 2B are a plan view and a cross-sectional view for explaining a manufacturing method of a GaN-based light emitting diode according to the first embodiment of the invention;

Figs. 3A and 3B are a plan view and a cross-sectional view for explaining the manufacturing method of the GaN-based light emitting diode according to the first embodiment of the invention;

Figs. 4A and 4B are a plan view and a cross-sectional view for explaining the manufacturing method

of the GaN-based light emitting diode according to the first embodiment of the invention;

Figs. 5A and 5B are a plan view and a cross-sectional view for explaining the manufacturing method of the GaN-based light emitting diode according to the first embodiment of the invention;

Fig. 6 is a plan view showing an array of openings formed in a mask in the manufacturing method of the GaN-based light emitting diode according to the first embodiment of the invention;

Fig. 7 is a scanning electron microscopic photograph of the surface configuration of a GaN-processed substrate immediately after formation of a light emitting element structure in the manufacturing method of the GaN-based light emitting diode according to the first embodiment of the invention;

Fig. 8 is a scanning electron microscopic photograph of the surface configuration of a GaN-processed substrate immediately after formation of a light emitting element structure in a manufacturing method of a GaN-based compound light emitting diode taken for comparison with the first embodiment of the invention;

Fig. 9 is a scanning electron microscopic photograph of the surface configuration of a GaN-processed substrate immediately after formation of a light emitting element structure in the manufacturing

method of the GaN-based light emitting diode according to the first embodiment of the invention;

Fig. 10 is a scanning electron microscopic photograph of the surface configuration of a GaN-processed substrate immediately after formation of a light emitting element structure in the manufacturing method of the GaN-based light emitting diode according to the first embodiment of the invention;

Fig. 11 is a cross-sectional view showing distribution of crystalline defects introduced in the process of growing GaN-based semiconductor layers forming the light emitting element structure in the manufacturing method of the GaN-based semiconductor light emitting diode according to the first embodiment of the invention;

Fig. 12 is a cross-sectional view showing an aspect of emission from the GaN-based light emitting diode manufactured by the first embodiment of the invention;

Fig. 13 is a cross-sectional view showing a GaN-based light emitting diode according to the second embodiment of the invention;

Fig. 14 is perspective view of the GaN-based light emitting diode according to the second embodiment of the invention, taken from the side of its n-side electrode;

Fig. 15 is a perspective view showing an image

display device according to the third embodiment of the invention;

Figs. 16A and 16B are a plan view and a cross-sectional view showing a GaN-based light emitting diode according to the fifth embodiment of the invention;

Figs. 17A and 17B are a plan view and a cross-sectional view showing a GaN-based light emitting diode according to the sixth embodiment of the invention;

Figs. 18A and 18B are a plan view and a cross-sectional view showing a GaN-based light emitting diode according to the seventh embodiment of the invention;

Figs. 19A and 19B are a plan view and a cross-sectional view showing a GaN-based light emitting diode according to the eighth embodiment of the invention;

Figs. 20A and 20B are a plan view and a cross-sectional view showing a GaN-based light emitting diode according to the ninth embodiment of the invention; and

Figs. 21A and 21B are a plan view and a cross-sectional view showing a GaN-based light emitting diode according to the tenth embodiment of the invention.

Best Mode for Carrying Out the Invention

Embodiments of the invention are explained below with reference to the drawings. In all figures showing embodiments of the invention, common or equivalent components are labeled common reference numerals.

Figs. 2A and 2B through Figs 5A and 5B show a

manufacturing method of a GaN-based light emitting diode according to the first embodiment of the invention, in which the figures numbered with the suffix A are plan views whereas the figures numbered with the suffix B are cross-sectional views.

In the first embodiment, first referring to Figs. 2A and 2B, a sapphire substrate 11 having a C+ oriented major surface, for example, is prepared. After the surface of the sapphire substrate 11 is cleaned by thermal cleaning, for example, an n-type GaN layer 12 doped with an n-type impurity such as Si is grown on the sapphire substrate 11 by metal organic chemical vapor deposition (MOCVD), for example. The n-type GaN layer 12 is desirably minimized in crystal defects and penetrating dislocations, and a thickness around 2 μm will be enough in most cases. Various techniques are employable for forming a defects-reduced n-type GaN layer 12. A typical technique first grows a GaN buffer layer or an AlN buffer layer (not shown) on the sapphire substrate 11 at a low temperature around 500°C, then raises the temperature to approximately 1000°C to crystallize it, and grows the n-type GaN layer 12 thereon. This technique may be modified to grow an undoped GaN layer after the growth of the GaN buffer layer or the AlN buffer layer and to thereafter grow the n-type GaN layer 12.

In the next step, a SiO_2 film, approximately 200

nm, for example, and a SiN film (especially, Si_3N_4 film), approximately 10 nm thick, are formed sequentially on the entire surface of the n-type GaN layer 12 by CVD, vacuum evaporation, sputtering, or the like, or preferably by plasma CVD. After that, a resist pattern (not shown) of a predetermined geometry is formed thereon by lithography. Then, under the existence of this resist pattern as a mask, the SiN film and the SiO_2 film are etched and patterned to a growth mask 14 having openings 13 at positions for forming elements by wet etching using a fluoric acid-based etchant, for example, or by RIE using an etching gas containing fluorine, such as CF_4, CFH_3, or the like. Each opening has the shape of a hexagon having one side normal to the <1-100> or <11-20> orientation. Size D of the openings is determined to meet the requirement. Usually, it is 2 to 13 μm. In this embodiment, it may be 3 μm, for example. Figs. 2A and 2B illustrate only one opening 13. Actually, however, a plurality of openings are formed in an array. Fig. 6 shows an exemplary layout of the openings 13. In Fig. 6, P denotes the pitch of the openings. The pitch P is 10 μm or more in most cases. In this embodiment, it may be 14 μm, for example.

In the next step, as shown in Figs. 3A and 3B, the n-type GaN layer 15, doped with an n-type impurity such as Si, is selectively grown on the n-type GaN

layer 12 exposed through the openings 13 in the growth mask 14. Growth temperature in this process may be 940°C. Growth rate is set very high, for example, as high as 11.0 to 11.3 μm/h, in planar growth reduction. In the process of this selective growth, the growth rate may be lowered by lowering the growth temperature than 940°C to render the growth slower near the interface with the n-type GaN layer 12. However, for the growth of the most part excluding the proximity to the interface with the n-type GaN layer 12, the growth temperature is set to 940°C, and the growth rate is raised to the high rate of 11.0 to 11.3 μm/h in planar growth reduction. As a result of this selective growth, the six-sided steeple-shaped n-type GaN layer 15 is obtained. Each of the six planes of the steeple-shaped n-type GaN layer 15 is composed of a plurality of (typically, a lot of, or innumerable) crystal planes inclined from the major surface of the sapphire substrate 11 by different angles of inclination from each other. However, assume here that each of the six planes is composed of four crystal planes F_1, F_2, F_3 and F_4 and they make a convex inclined crystal plane as a whole. In this case, angles of inclination of the crystal planes F_1, F_2, F_3 and F_4 become smaller from the bottom of the n-type GaN layer 15 toward its apex. Angle of inclination of the crystal plane F_4 of the upper most portion including the apex is, for example,

62° to 63° whereas angle of inclination of the crystal plane F_1 of the lowermost portion including the bottom is, for example, 74° to 82°. All of the crystal planes composing the generally convex inclined crystal plane can be regarded as S-oriented planes or substantially S-oriented planes. Accordingly, the n-type GaN layer 15 is a combination of a plurality of single crystals slightly different in crystalline orientation from each other. Size of the n-type GaN layer 15 may be determined depending upon the requirement. In this case, however, it is larger than the size of the opening 13. More specifically, it is approximately three times the size of the opening 15.

Subsequently to the growth of the n-type GaN layer 15 as explained above, as shown in Figs. 4A and 4B, an active layer 16 of InGaN compounds, for example, and a p-type GaN layer 17 doped with a p-type impurity such as Mg are sequentially grown on the sapphire substrate 11. As a result, the six-sided steeple-shaped n-type GaN layer 15 as well as the active layer 16 and the p-type GaN layer 17 grown on the inclined crystal planes of the n-type GaN layer 15 make a light emitting diode structure having double hetero structure. After that, Mg in the p-type GaN layer 17 is activated by annealing in a nitrogen atmosphere controlled at a temperature around 850°C. Thickness of the active layer and the p-type GaN layer 17 is

determined depending upon the requirement. However, thickness of the active layer 16 is preferably 3 nm for example (thickness of the active layer 16 after growth usually has some small measure of distribution from the top to the bottom). Thickness of the p-type GaN layer 17 is preferably as thin as possible within the extent adversely affecting the emission property. For example, it may be 0.2 μm. If it is 0.05 μm, the operation voltage can be reduced to 3 V or less. Growth temperatures of these GaN-based semiconductor layers are controlled in the range of 650 to 800°C, more specifically at 740°C for example, in case of the active layer 16. In case of the p-type GaN layer 17, growth temperature is set to a rather high temperature within the extent not adversely affecting the property of the active layer 16, namely in the range of 880 to 940°C, and more specifically at 900°C, for example. The active layer 16 may be composed of either a single layer of InGaN, for example, or a multi-quantum well structure alternately stacking two InGaN layers different in In composition, for example. The In composition is determined depending upon the intended emission wavelength. In the p-type GaN layer 17, Mg concentration of its uppermost layer is preferably increased to assure good ohmic contact with a p-side electrode, explained later. Alternatively, a p-type InGaN layer doped with Mg as a p-type impurity, for

example, and easy to make ohmic contact may be grown on the p-type GaN layer 17, and the p-side electrode may formed thereon.

Size W of the light emitting structure is approximately 10 μm for example (see Fig. 4B).

With regard to source materials for growth of the above-explained GaN-based semiconductor layers, here are used, for example, trimethylgallium ($(CH_3)_3Ga$, TMG) as the source material of Ga, trimethylaluminum ($(CH_3)_3Al$, TMA) as the source material of Al, trimethylindium ($(CH_3)_3In$, TMI) as the source material of In and NH_3 as the source material of N. Concerning the dopants, here are used silane (SiH_4) as the n-type dopant, and bis(methyl cyclopentadienile)-magnesium ($(CH_3C_5H_4)_2Mg$) or bis(cyclopentadienile)-magnesium ($(C_5H_5)_2Mg$) as the p-type dopant.

Regarding the carrier gas atmosphere during growth of the GaN-based semiconductor layers, a mixed gas of N_2 and H_2 is used for the n-type GaN layer 12 and the n-type GaN layer 15. For growth of the active layer 16, a N_2 gas atmosphere is used as the carrier gas atmosphere. For growth of the p-type GaN layer 17, a mixed gas of N_2 and H_2 is used. In this case, since the N_2 gas is used as the carrier gas atmosphere during growth of the active layer 16 and the carrier gas atmosphere does not contain H_2, it is possible to prevent elimination of In and deterioration of the

active layer 16 thereby. Moreover, since the mixed gas atmosphere of N_2 and H_2 is used as the carrier gas atmosphere for growth of the p-type GaN layer 17, the p-type layer can be grown with a good crystallographic quality.

After that, the sapphire substrate 11 having GaN-based semiconductor layers grown thereon is removed from the MOCVD apparatus.

In the next step, a Ni film, Ag film (or Pt film) and Au film are sequentially deposited on the entire substrate surface by vacuum evaporation, for example. After that, a resist pattern of a predetermined geometry is formed on them by lithography. Under the existence of the resist pattern as a mask, the Ni film, Ag film and Au film are etched. As a result, a Ni/Ag(or Pt)/Au structured p-side electrode 18 is formed in the region including the apex of the active layer 16 and the p-type GaN layer 17 grown on the six-sided steeple-shaped n-type GaN layer 15. Size of the p-side electrode 18 is determined to minimize the flow of the drive current in the defective region in the n-type GaN layer 15 and others. More specifically, it may be approximately 4 μm.

In the next step, the growth mask 14 is selectively removed by etching to expose the n-type GaN layer 12. Thereafter, a Ti film, Pt film and Au film are sequentially deposited on the entire substrate

surface by vacuum evaporation, and a resist pattern of a predetermined geometry is formed thereon by lithography. Thereafter, under the existence of the resist pattern as a mask, the Ti film, Pt film and Au film are etched. As a result, a Ti/Pt/Au structured n-side electrode 19 if formed in contact with the n-type GaN layer 12.

After that, the substrate having an array of light emitting diode structures thereon is divided to chips by etching or exfoliation with a dicer or excimer laser to obtain the intended GaN-based light emitting diode. The substrate may undergo an additional process of approximately leveling its surface before the substrate having the array of light emitting diode structures is divided to chips.

The GaN-based light emitting diode, thus obtained, was driven for trial by supplying a current between the p-side electrode 18 and the n-side electrode 19. As a result, emission through the sapphire substrate 11 was confirmed at an emission wavelength in the range from 380 to 620 nm, for example, at the emission wavelength of 450 nm, depending upon the In composition of the active layer. Emission efficiency was high, and the emission output was 40 μW under the drive current of 200 μA, for example.

Here is explained the angle of inclination of the

crystal plane F_1 among the plurality of crystal planes composing each convex inclined crystal plane of the six-sided steeple-shaped n-type GaN layer 15 in relation to the emission efficiency. As already explained, the angle of inclination of the crystal plane F_1 is 74° to 82°, for example. Emission efficiency tends to become better as the angle of inclination increases. For example, in case the angle of inclination is 74°, when the growth thickness of the n-type GaN layer 15 is 2 μm in planar growth reduction, under the size D of the opening 13 being D=10 μm and the pitch P being 29 μm, emission efficiency was 100 m/W/A. In case of 76°, when the growth thickness of the n-type GaN layer 15 is 2 μm in planar growth reduction, under the size D of the opening 13 being D=3 μm and the pitch P is P=17 μm, the emission efficiency was 200 mW/A. In case of 82°, when the growth thickness of the n-type GaN layer 15 is 4 μm in planar growth reduction, under the size D of the opening 13 being D=3 μm and the pitch P is P=17 μm, the emission efficiency was 210 mW/A.

Next explained is the size D and the pitch P of the openings 13 in the growth mask 14 shown in Fig. 6 in relation to the emission efficiency. Many samples with combinations (D, P) (in μm) were prepared while changing D in the range from 3 to 10 μm and P in the range from 11~28 μm, and the n-type GaN layer 15 was

selectively grown on individual samples. As a result, there was the tendency that the larger the pitch P, the better the inclined crystal planes of the steeple-shaped n-type GaN layer 15 and the higher the emission efficiency. Regarding the size D, there was the tendency that the smaller the size D the higher the emission efficiency. Additionally, it was observed how the light was extracted, and much light appeared to emit from the entirety, not only from the central portion of the element but also from the side surfaces.

Fig. 7 shows a photograph of the six-sided steeple-shaped n-type GaN layer 15 taken by a scanning electron microscope (SEM). The size D of the opening 13 in the growth mask 14 is 3 μm, and the pitch P is 10 μm. For comparison, Fig. 8 shows a SEM photograph of a conventional six-sided pyramidal n-type GaN layer having S-oriented inclined crystal planes. Size D of the opening 13 in the growth mask 14 is 10 μm, and pitch P is 29 μm.

In addition, Fig. 9 shows a SEM photograph of an n-type GaN layer 15 in case of the size D of the opening 13 in the growth mask 14 being 3 μm and the pitch P being approximately 17 μm. Fig. 10 shows a SEM photograph of an n-type GaN layer 15 in case of the size D of the opening 13 in the growth mask 14 being 3 μm and the pitch P being approximately 28 μm (note that the scale is 1/2 of Fig. 9). It is appreciated from

Figs. 9 and 10 that the six-sided steeple-shaped n-type GaN layer 15 has a higher angle of inclination near the growth mask 14 in case the pitch P is approximately 28 μm than in case it is approximately 17 μm.

According to the first embodiment, the following various advantages can be obtained.

As shown in Fig. 11, while the n-type GaN layer 15 grows, dislocations 20 and depositional defects 21 therein. Some of them extend across the active layer 16, but they disappear at least in the portion close to the apex of the n-type GaN layer 15. Considering it, the first embodiment determines the size of the p-side electrode so that a drive current supplied between the p-side electrode 18 and the n-side electrode 19 does not flow the defective regions in the n-type GaN layer 15 and others. Therefore, the first embodiment can provide a GaN-based light emitting diode remarkably enhanced in emission efficiency and excellent in reliability as well.

Further, the first embodiment grows the six-sided steeple-shaped n-type GaN layer 15 each composed of a plurality of crystal planes (F_1, F_2, F_3 and F_4) inclined from the major surface of the sapphire substrate 11 by different angles of inclination from each other to exhibit a convex crystal plane as a whole, and grows the active layer 16 and the p-type GaN layer 17 thereon. Thereby, the p-type GaN layer 17 also has

inclined crystal planes similar to those of the n-type GaN layer 15. Therefore, when a drive current is supplied between the p-side electrode 18 and the n-side electrode 19, part of light toward the p-type GaN layer 17 in the light emitted from the active layer 16 is reflected at the outer surface of the p-type GaN layer 17 and travels toward the sapphire substrate 11. On the other hand, part of the light toward inside the n-type GaN layer 15 in the light emitted from the active layer 16 directly travels toward the sapphire substrate 11. As a result, the first embodiment can efficiently extract the light externally from the active layer 16 through the sapphire substrate 11, and can enhance the emission efficiency (see Fig. 12).

Moreover, in the GaN-based light emitting diode according to the first embodiment, the area occupied by each element can be made very small as compared with the conventional GaN-based light emitting diode shown in Figs. 1A and 1B. For example, while the size of the six-sided pyramidal light emitting element structure of the conventional GaN-based light emitting diode is approximately 20 μm, the size of the six-sided steeple-shaped light emitting element structure of the GaN-based light emitting diode according to the first embodiment is much smaller, namely 10 μm approximately.

Furthermore, since the first embodiment uses the Ni/Ag/Au structure including Ag having a high

reflectance as the p-side electrode 18, the first embodiment can enhance the reflectance of the upper part of the six-sided steeple-shaped p-type GaN layer 17, where the p-side electrode 18 is formed. Thereby, the first embodiment can further enhance the light extracting efficiency and can further enhance the emission efficiency.

In addition, according to the first embodiment, the light extracting direction can be made closer to the direction normal to the substrate surface. That is, distribution of emission from a light emitting element on a plane is usually called Lambertian, or called complete diffusion plane as well. In this case, emission is isotropic from all directions. However, if a black mask, or the like, is provided, light travels also toward the black mask. Therefore, to extract light forward, a lens is required. The first embodiment, however, can control the light extracting direction only by controlling the growth.

Next explained is a GaN-based light emitting diode according to the second embodiment of the invention.

In the second embodiment, after the layers are grown up to the p-type GaN layer 17 by the same steps as those of the first embodiment, the p-side electrode 18 is formed on the p-type GaN layer 17. After that, the n-type GaN layer 12 and other upper layers are

exfoliated from the sapphire substrate by irradiating a laser beam from the bottom of the sapphire substrate 11 with an excimer laser. Thereafter, the bottom surface of the exfoliated n-type GaN layer 12 is smoothed by etching, for example, and the n-side electrode 19 is formed on the smoothed bottom surface of the n-type GaN layer 12 as shown in Fig. 13. The n-side electrode 19 may be a transparent electrode made of ITO, for example. In this case, the n-side electrode 19 can be formed to lie over the wide area on the bottom surface of the n-type GaN layer 12 including the area under the six-sided steeple-shaped structure. In case the n-side electrode 19 is a Ti/Pt/Au structured metal laminated film, an opening 19a is provided in the n-side electrode 19 in alignment with the six-sided steeple-shaped n-type GaN layer 15 as shown in Fig. 14 to permit light to go out through the n-type GaN layer 12.

The second embodiment assures the same advantages as those of the first embodiment.

Next explained is an image display device according to the third embodiment of the invention. Fig. 15 shows the image display device.

As shown in Fig. 15, the image display device includes GaN-based light emitting diodes regularly aligned in the orthogonal x and y directions in a plane of a sapphire substrate 11 to make a two-dimensional array of GaN-based light emitting diodes. Structure of

each GaN-based light emitting diode may be identical to that of the first embodiment, for example.

In the y direction, GaN-based light emitting diodes for emitting red (R), GaN-based light emitting diodes for emitting green (G) and GaN-based light emitting diodes for emitting blue (B) are aligned in a close relation, and three GaN-based light emitting diodes for different colors compose one pixel. Individual p-side electrodes 18 of GaN-based light emitting diodes for red aligned in the x direction are connected to each other by wiring 22. Similarly, p-side electrodes 18 of the GaN-based light emitting diodes for green aligned in the x direction are connected to each other by wiring 23, and p-side electrodes 18 of the GaN-based light emitting diodes for blue aligned in the x direction are connected to each other by wiring 24. On the other hand, n-side electrodes 19 extend in y directions and each functions as a common electrode of a series of GaN-based light emitting diodes aligned in the y direction.

The simple-matrix image display device having the above-explained configuration can display an image by selecting the wirings 22 to 24 and the n-side electrodes 19 depending upon a signal of an image to be displayed, thereby supplying a current to the selected GaN-based light emitting diodes of the selected pixel to drive them to emit light.

According to the third embodiment, each GaN-based light emitting diode has the same configuration as that of the first embodiment and therefore has high emission efficiency. Thus, a high-luminance full-color image display device can be realized.

Next explained is an illuminating device according to the fourth embodiment of the invention. The illuminating device has the same configuration as the image display device shown in Fig. 15.

The illuminating device can emit illuminating light by selecting the wirings 22 to 24 and the n-side electrodes 19 depending upon the color of the illuminating light, thereby supplying a current to the selected GaN-based light emitting diodes of the selected pixel to drive them to emit light.

According to the fourth embodiment, each GaN-based light emitting diode has the same configuration as that of the first embodiment and therefore has high emission efficiency. Thus, a high-luminance full-color illuminating device can be realized.

Next explained is a GaN-based light emitting diode according to the fifth embodiment of the invention. This GaN-based light emitting diode is illustrated in Figs. 16A and 16B.

In the fifth embodiment, the GaN-based semiconductor diode is manufactured in the same manner as the first embodiment. However, the fifth embodiment

is different from the first embodiment in that the size D of the opening 13 in the growth mask 14 is D=10 μm and the pitch P is P=28 μm.

According to the fifth embodiment, since the opening in the growth mask 14 has the relatively small size D=10 μm, it diminishes the region liable to generate dislocations 20 and depositional defects 21 during selective growth of the n-type GaN layer 15, and thereby reduces adverse influence of these crystal defects to emission of light. As a result, a GaN-based light emitting diode enhanced in emission efficiency and reliability can be obtained. For example, when the drive current is 200 μA, emission output of 25 μW is obtained. In addition, the fifth embodiment ensures the same advantages as those of the first embodiment.

Next explained is a GaN-based light emitting diode according to the sixth embodiment of the invention. Figs. 17A and 17B show this GaN-based light emitting diode.

In the sixth embodiment, the growth mask 14 having openings 13 is formed in the same manner as the first embodiment. However, unlike the first embodiment, the size D of the opening 13 is D=10 μm, and the pitch P is P=28 μm. Then, under the existence of this growth mask 14, the n-type GaN layer 15 is selectively grown. In this process, the growth temperature is set at 1020°C, for example, and the

growth rate is set to 4 μm/h in planar growth reduction. In the process of this selective growth, the growth rate may be lowered by lowering the growth temperature than 1020°C to render the growth slower near the interface with the n-type GaN layer 12. However, for the growth of the most part excluding the proximity to the interface with the n-type GaN layer 12, the growth temperature is raised to 1020°C, and the growth rate is raised to 4 μm/h in planar growth reduction. After that, the growth is continued at the lower growth rate of 0.5 μm/h. As a result, the steeple-shaped n-type GaN layer 15 grows with inclined crystal planes each exhibiting a convex plane as a whole as shown in Figs. 17A and 17B. In this case, the inclined crystal planes comprise M-oriented or less inclined crystal planes formed on side surfaces of the lower part of the n-type GaN layer 15 and S-oriented planes formed on side surfaces of the upper part of the n-type GaN layer 15.

After that, the process is continued in the same manner as the first embodiment, and the GaN-based light emitting diode shown in Figs. 17A and 17B is completed. In this case, size W of the light emitting element is W=13 μm.

According to the sixth embodiment, the same advantages as those of the first and second embodiments can be obtained. For example, when the drive current

is 200 μA, emission output of 25 μW is obtained.

Next explained is a GaN-based light emitting diode according to the seventh embodiment of the invention. Figs. 18A and 18B illustrate this GaN-based light emitting diode.

In the seventh embodiment, the growth mask 14 having openings 13 is formed in the same manner as the first embodiment. However, size D of the opening 13 is D=10 μm, and the pitch P is P=28 μm. Subsequently, similarly to the first embodiment, the n-type GaN layer 15 is selectively grown under the existence of the growth mask 14, and the active layer 16 and the p-type GaN layer 17 are grown thereon. In this embodiment, the active layer 16 has a MQW structure composed of a barrier layer 16a, well layer 16b, barrier layer 16c, well layer 16d and barrier layer 16e. The barrier layer 16a, well layer 16b, barrier layer 16c, well layer 16d and barrier layer 16e may be InGaN layers, for example. In this case, size W of the light emitting structure is W=13 μm.

After that, the process is continued similarly to the first embodiment to complete the GaN-based light emitting diode shown in Figs. 18A and 18B.

According to the seventh embodiment, the same advantages as those of the first and second embodiments can be obtained. For example, when the drive current is 200 μA, emission output of 80 μW is obtained.

Next explained is a GaN-based light emitting diode according to the eighth embodiment of the invention. Figs. 19A and 19B illustrate this GaN-based light emitting diode.

In the eighth embodiment, the growth mask 14 having openings 13 is formed in the same manner as the first embodiment. However, unlike the first embodiment, the size D of the opening 13 is D=10 μm, and the pitch P is P=28 μm. Then, under the existence of this growth mask 14, the n-type GaN layer 15 is selectively grown. In this process, the growth temperature is set at 940°C, for example, and the growth rate is set at a very high rate of 11.0 to 11.3 μm/h in planar growth reduction. In the process of this selective growth, the growth rate may be lowered by lowering the growth temperature than 940°C to render the growth slower near the interface with the n-type GaN layer 12. However, for the growth of the most part excluding the proximity to the interface with the n-type GaN layer 12, the growth temperature is raised to 940°C, and the growth rate is raised to the very high rate of 11.0 to 11.3 μm/h in planar growth reduction. After that, the growth is continued at the lower growth rate of 0.5 μm/h. As a result, the steeple-shaped n-type GaN layer 15 grows in form of a six-sided frustum-shaped steeple having the inclined crystal planes each exhibiting a convex plane as a whole and having a C-

oriented or quasi-C-oriented crystal plane on the top of the apex portion as shown in Figs. 19A and 19B. Subsequently, an undoped GaN layer 22 is grown to a thickness around 100 nm to close the six-sided pyramid on the apex portion of the n-type GaN layer 15 at the growth temperature of 940°C, for example and the growth rate of 11.0 to 11.3 μm/h. The undoped GaN layer 22 serves as a current-blocking region.

After that, the process is continued in the same manner as the first embodiment to complete the GaN-based light emitting diode shown in Figs. 19A and 19B. In this case, size W of the light emitting structure is W=13 μm.

According to the eighth embodiment, the same advantages as those of the first and second embodiments can be obtained. Especially, since the undoped GaN layer 22 serves as a current-blocking region and can prevent a drive current from flowing through crystallographically inferior regions, the eighth embodiment attains greater emission efficiency. For example, when the drive current is 200 μA, emission output of 80 μW is obtained.

Next explained is a GaN-based light emitting diode according to the ninth embodiment of the invention. Figs. 20A and 20B illustrate this GaN-based light emitting diode.

In the ninth embodiment, the growth mask 14

having openings 13 is formed in the same manner as the first embodiment. However, unlike the first embodiment, the opening 13 has the form of an elongated hexagon that may have, for example, the maximum size of 30 μm, minimum size of 10 μm in the direction normal to the direction of the maximum size and the pitch P of 28 μm. Then, under the existence of this growth mask 14, the n-type GaN layer 15 is selectively grown. In this process, the growth temperature is set at 940°C, for example, and the growth rate is set at a very high rate of 11.0 to 11.3 μm/h in planar growth reduction. In the process of this selective growth, the growth rate may be lowered by lowering the growth temperature than 940°C to render the growth slower near the interface with the n-type GaN layer 12. However, for the growth of the most part excluding the proximity to the interface with the n-type GaN layer 12, the growth temperature is raised to 940°C, and the growth rate is raised to the very high rate of 11.0 to 11.3 μm/h in planar growth reduction. As a result, in a cross-sectional view taken along the direction of the minimum size of the opening in the growth mask 14, the steeple-shaped n-type GaN layer 15 grows to expand in the direction normal to the cross section and include inclined crystal planes each exhibiting a convex plane as a whole, as shown in Figs. 20A and 20B.

After that, the process is continued in the same

manner as the first embodiment to complete the GaN-based light emitting diode shown in Figs. 20A and 20B. In this case, size W of the light emitting structure is W=13 μm.

According to the ninth embodiment, the same advantages as those of the first and second embodiments can be obtained. For example, when the drive current is 200 μA, emission output of 80 μW is obtained.

Next explained is a GaN-based light emitting diode according to the tenth embodiment of the invention. Figs. 21A and 21B illustrate this GaN-based light emitting diode.

In the tenth embodiment, the growth mask 14 having openings 13 is formed in the same manner as the first embodiment. However, unlike the first embodiment, the size D of the opening 13 is D=10 μm, and the pitch P is P=28 μm. Then, under the existence of this growth mask 14, the n-type GaN layer 15 is selectively grown. In this process, the growth temperature is set at 940°C, for example, and the growth rate is set at a very high rate of 11.0 to 11.3 μm/h in planar growth reduction. In the process of this selective growth, the growth rate may be lowered by lowering the growth temperature than 940°C to render the growth slower near the interface with the n-type GaN layer 12. However, for the growth of the most part excluding the proximity to the interface with the n-

type GaN layer 12, the growth temperature is raised to 940°C, and the growth rate is raised to the very high rate of 11.0 to 11.3 μm/h in planar growth reduction.

After that, the growth mask is removed by wet etching using a fluoric acid-based etchant, for example, or by RIE using an etching gas containing fluorine, such as CF_4, CFH_3, or the like.

Thereafter, an n-type GaN layer (not shown) is grown to a thickness around 1 μm, for example, at the growth temperature of 960°C, for example. Consecutively, the active layer 16 and the p-type GaN layer 17 are grown on the clean surface of the n-type GaN layer. In this case, size W of the light emitting structure is W=13 μm.

After that, the process is continued in the same manner as the first embodiment up to the p-side electrode 18.

Subsequently, a resist pattern (not shown) is formed by lithography to cover the p-type GaN layer 17 in the region excluding the region for forming the n-side electrode. Under the resist pattern as a mask, the p-type GaN layer 17 and the active layer 16 are selectively removed by etching by RIE, for example, to make an opening and expose the n-type GaN layer 12 through the opening. Thereafter, the resist pattern is removed. Then, a Ti film, Pt film and Au film are formed sequentially on the entire substrate surface by

vacuum evaporation, for example, and a resist pattern of a predetermined geometry is formed thereon by lithography. Under the resist pattern as a mask, the Ti film, Pt film and Au film are etched. As a result, the n-side electrode 19 of the Ti/Pt/Au structure is formed in contact with the n-type GaN layer 12 through the opening formed in the p-type GaN layer 17 and the active layer 16.

According to the tenth embodiment, the same advantages as those of the first and second embodiments can be obtained. For example, when the drive current is 200 μA, emission output of 25 μW is obtained.

In addition, the tenth embodiment has the following advantages. As already explained, the conventional GaN-based light emitting diode needs the process of selectively growing the six-sided pyramidal n-type GaN layer having inclined crystal planes inclined from the major surface of the substrate on the n-type GaN layer exposed through the opening in the growth mask of silicon oxide (SiO_2) or silicon nitride (SiN); and the process of growing the active layer, p-type GaN layer and others on the inclined crystal plane under the existence of the growth mask retained. However, since the selective growth of the n-type GaN layer and the later growth of the p-type GaN layer are carried out at a high temperature of 900°C or more, there may arise the phenomenon that silicon (Si) and

oxygen (O) are eliminated from the surface of the growth mask and incorporated into layers grown near around during the growth. Adverse influences of this phenomenon are especially serious during the growth of the p-type GaN layer. It has been found that if Si workable as an n-type impurity of GaN is incorporated into the p-type GaN layer while it grows, the intended p-type is difficult to obtain and that even if a p-type is obtained, both the hole concentration and the mobility seriously decrease, thereby disturbing enhancement of the emission efficiency of the light emitting diode. Further, the conventional GaN-based light emitting diode needs the process of lithography for making the opening in the growth mask, and this process needs the process of bringing the resist into close contact with the mask surface to locally remove it. In this removal process, however, the resist is liable to remain in minute gaps of the growth mask and very difficult to remove. In later growth at a high temperature, any residual resist may become an impurity source and may deteriorate the property of a p-type GaN layer, or the like. In contrast, in the tenth embodiment, since the growth mask 14 is removed by etching before the growth of the active layer 16 and the p-type GaN layer 17, the growth mask 14 does not exist when the active layer 16 and the p-type GaN layer 17 are grown. Thus, the tenth embodiment is free from

the problem of undesirable incorporation of Si from the growth mask 14 into layers grown thereon, and free from the problem of contamination by the resist. Therefore, the tenth embodiment assures the growth of a sufficiently Mg-doped and low-resistant p-type GaN layer 17, and enables further enhancement of the emission efficiency of the GaN light emitting diode.

Heretofore, specific embodiments of the invention have been explained. However, the invention is not limited to these embodiments but contemplated various changes and modifications based on the technical concept of the invention.

For example, numerical values, materials, structures, shaped, substrates, source materials, processes, and so on, which have been raised in the explanation of the first to tenth embodiments are nothing but examples, and other numerical values, materials, structures, shaped, substrates, source materials, processes, and so on, may be used where necessary.

More specifically, to enhance the property of the active layer 16 in the first to tenth embodiment, for example, an AlGaN layer excellent in light confinement property may be formed near the active layer 16, and/or an InGaN layer having a small In composition, for example, may be formed. If an effect of diminishing the band gap by so-called bowing is desirable, Al is

added to InGaN to make AlGaInN. Moreover, an optical guide layer may be interposed between the active layer 16 and the n-type GaN layer 12 and/or between the active layer 16 and the p-type GaN layer 17, if necessary.

Although the first to tenth embodiments use a sapphire substrate, any other substrate such as a SiC substrate, Si substrate, or the like, may be used where appropriate. Alternatively, a GaN substrate made by a lateral crystal growth technique such as ELO (Epitaxial Lateral Overgrowth) or Pendeo may be used.

In the first to tenth embodiments, a contact metal layer of Ni, Pd, Co, Sb, or the like, having a thickness equal to or larger than the wavelength permitting penetration of light generated in the active layer 16 may be interposed between the p-type GaN layer 17 and the p-side electrode 18. In this case, the effect of enhancing reflection by the contact metal layer further enhanced the emission efficiency of the GaN-based light emitting diode.

In the third and fourth embodiments, a plurality of GaN-based light emitting diodes are monolithically formed on the sapphire substrate. However, the GaN-based light emitting diodes monolithically formed on the sapphire substrate 11 may be divided to discrete elements, then mounted in the same layout as the third and fourth embodiments on a base and connected by

wirings in the same configuration as explained before.

As described above, according to the invention, the semiconductor layer of the first conduction type is formed on a major surface to include a convex crystal portion having an inclined crystal plane that comprises a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole, or an inclined crystal plane exhibiting a substantially convex plane as a whole. Then, at least on the inclined crystal plane, at least the active layer and the semiconductor layer of the second conduction type are deposited sequentially to make the light emitting element structure. Therefore, the invention can provide a semiconductor light emitting element, integrated semiconductor light emitting device, image display device and illuminating device, which are significantly enhanced in emission efficiency and small in occupied area per each element.

CLAIMS

1. A semiconductor light emitting element comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

2. The semiconductor light emitting element according to claim 1 wherein the crystal portion has a wurtzite crystal structure.

3. The semiconductor light emitting element according to claim 1 wherein the crystal portion is made of a nitride III-V compound semiconductor.

4. The semiconductor light emitting element

according to claim 1 wherein the semiconductor layer of the first conduction type, the active layer and the semiconductor layer of the second conduction type are made of nitride III-V compound semiconductors.

5. The semiconductor light emitting element according to claim 2 wherein the crystal planes composing the inclined crystal plane are S-oriented planes.

6. The semiconductor light emitting element according to claim 2 wherein the angles of inclination of the crystal planes composing the inclined crystal plane become stepwise smaller from the bottom of the crystal portion toward the apex thereof.

7. The semiconductor light emitting element according to claim 6 wherein the angle of inclination of the crystal plane including the apex in the plurality of crystal planes composing the inclined crystal plane is in the range from 60 degrees to 65 degrees.

8. The semiconductor light emitting element according to claim 1 wherein the crystal p0ortion is steeple-shaped.

9. The semiconductor light emitting element according to claim 1 wherein the crystal portion has a six-sided steeple configuration.

10. The semiconductor light emitting element according to claim 1 wherein the crystal portion is

elongate in a direction parallel to the major surface.

11. A method of manufacturing a semiconductor light emitting element having: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

12. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the growth mask is made of one or lamination of silicon nitride, silicon oxide nitride and silicon oxide.

13. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein at least the surface of the growth mask is made of silicon nitride.

14. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the size of the opening in the growth mask is in the range from 2 μm to 13 μm.

15. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the crystal portion has a wurtzite crystal structure.

16. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the crystal portion is made of a nitride III-V compound semiconductor.

17. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the semiconductor layer of the first conduction type, the first semiconductor layer, the second semiconductor

layer, the active layer and the semiconductor layer of the second conduction type are made of nitride III-V compound semiconductors.

18. The method of manufacturing a semiconductor light emitting element according to claim 14 wherein the crystal planes composing the inclined crystal plane are S-oriented planes.

19. The method of manufacturing a semiconductor light emitting element according to claim 15 wherein the angles of inclination of the crystal planes composing the inclined crystal plane become stepwise smaller from the bottom of the crystal portion toward the apex thereof.

20. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the crystal portion is steeple-shaped.

21. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the crystal portion has a six-sided steeple configuration.

22. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the crystal portion is elongate in a direction parallel to the major surface.

23. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein growth temperature for the selective growth is controlled in the range from 920°C to 960°C.

24. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein growth rate for the selective growth is controlled to be equal to or higher than 6 μm/h.

25. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein the growth temperature for the active layer and the semiconductor layer of the second conduction type is set lower than the growth temperature for selective growth of the second semiconductor layer.

26. The method of manufacturing a semiconductor light emitting element according to claim 11 wherein after the second semiconductor layer is selectively grown to have a crystal plane substantially parallel to the major surface on the top thereof, an undoped semiconductor layer is grown on the top of the second semiconductor layer.

27. The method of manufacturing a semiconductor light emitting element according to claim 11 further comprising:

a step of removing the growth mask between the step of selectively growing the second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask and the step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type.

28. An integrated semiconductor light emitting device including a plurality of integrated semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

29. A method of manufacturing an integrated semiconductor light emitting device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to

exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

30. The method of manufacturing an integrated semiconductor light emitting device according to claim 29 wherein the size of each opening in the growth mask is in the range from 4/1 to 1 time the size of each

semiconductor light emitting element.

31. The method of manufacturing an integrated semiconductor light emitting device according to claim 29 wherein the distance between nearest two of the openings is equal to or more than two times the size of each semiconductor light emitting element.

32. The method of manufacturing an integrated semiconductor light emitting device according to claim 29 wherein the size of each opening in the growth mask is in the range from 2 μm to 13 μm.

33. The method of manufacturing an integrated semiconductor light emitting device according to claim 29 wherein the distance between nearest two of the openings is equal to or more than 10 μm.

34. An image display device including a plurality of semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the

semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

35. A method of manufacturing an image display device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

36. An illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor

layer of the second conduction type.

37. A method of manufacturing an illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each including: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane composed of a plurality of crystal planes inclined from the major surface by different angles of inclination to exhibit a convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the

first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

38. A semiconductor light emitting element comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

39. A method of manufacturing a semiconductor light emitting element having: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially

convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

40. An integrated semiconductor light emitting device including a plurality of integrated semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type

which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

41. A method of manufacturing an integrated semiconductor light emitting device including a plurality of integrated semiconductor light emitting elements each having: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second

conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

42. An image display device including a plurality of semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the

semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

43. A method of manufacturing an image display device integrating a plurality of integrated light emitting elements each having a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having openings at predetermined positions on the first semiconductor layer;

a step of selectively growing a second

semiconductor layer of the first conduction type on the first semiconductor layer exposed through the openings in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor layer.

44. An illuminating device having a single semiconductor light emitting element or a plurality of integrated semiconductor light emitting elements each comprising:

a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole;

at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion;

a first electrode electrically connected to the semiconductor layer of the first conduction type; and

a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type.

45. A method of manufacturing an illuminating device having a single semiconductor light emitting element or

a plurality of integrated semiconductor light emitting elements each including: a semiconductor layer of a first conduction type which is formed on a major surface and includes a convex crystal portion having an inclined crystal plane exhibiting a substantially convex plane as a whole; at least an active layer and a semiconductor layer of a second conduction type which are sequentially layered at least on the inclined crystal plane of the crystal portion; a first electrode electrically connected to the semiconductor layer of the first conduction type; and a second electrode formed on the semiconductor layer of the second conduction type on the crystal portion and electrically connected to the semiconductor layer of the second conduction type, comprising:

a step of growing a first semiconductor layer of the first conduction type on a substrate;

a step of forming a growth mask having an opening at a predetermined position on the first semiconductor layer;

a step of selectively growing a second semiconductor layer of the first conduction type on the first semiconductor layer exposed through the opening in the growth mask; and

a step of sequentially growing at least the active layer and the semiconductor layer of the second conduction type to cover the second semiconductor

layer.

ABSTRACT

An n-type GaN layer is grown on a sapphire substrate, and a growth mask of SiN, for example, is formed thereon. On the n-type GaN layer exposed through an opening in the growth mask, a six-sided steeple-shaped n-type GaN layer is selectively grown, which has inclined crystal planes each composed of a plurality of crystal planes inclined from the major surface of the sapphire substrate by different angles of inclination to exhibit a convex plane as a whole. On the n-type GaN layer, an active layer and a p-type GaN layer are grown to make a light emitting element structure. Thereafter, a p-side electrode and an n-side electrode are formed.

Fig. 1A

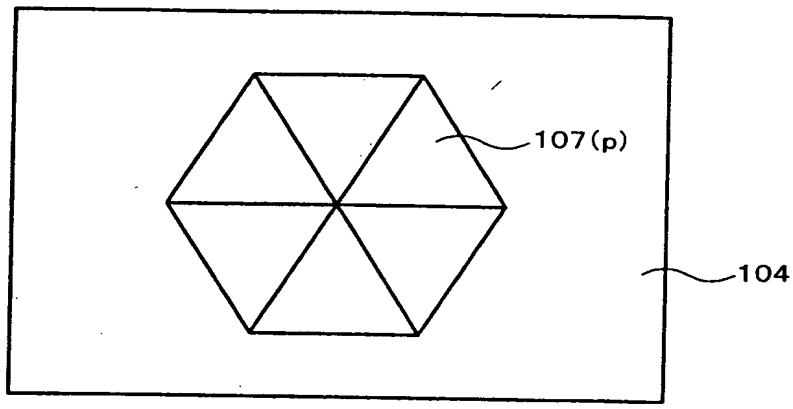

Fig. 1B

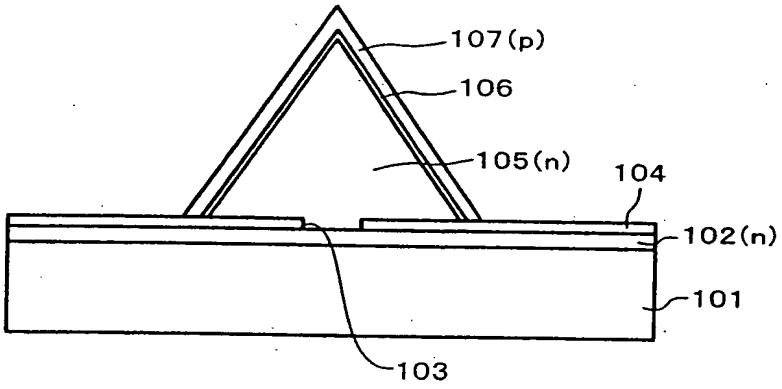

Fig. 2A

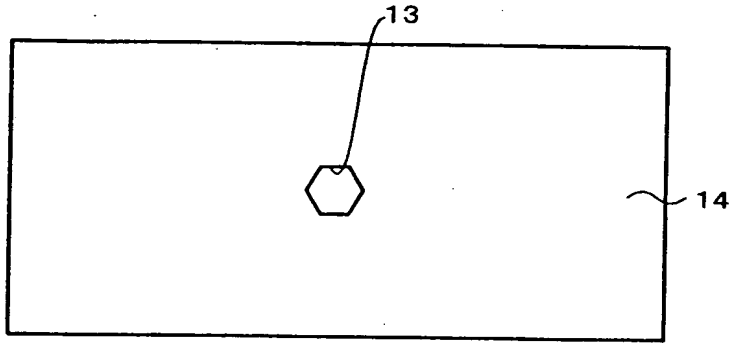

Fig. 2B

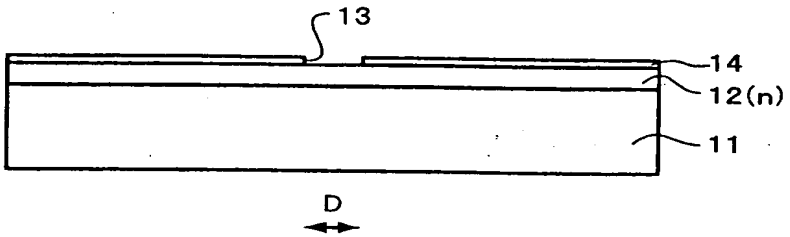

Fig. 3A

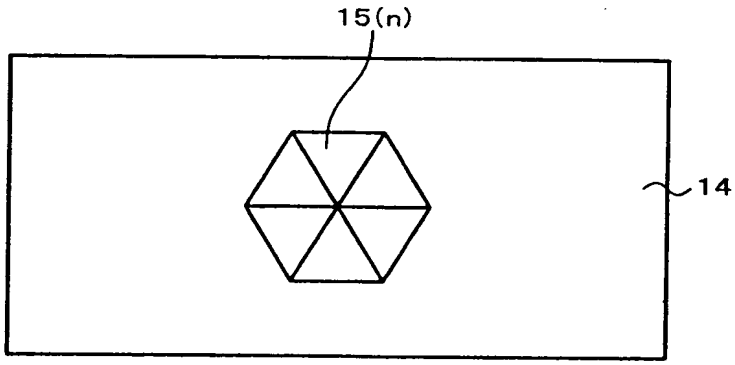

Fig. 3B

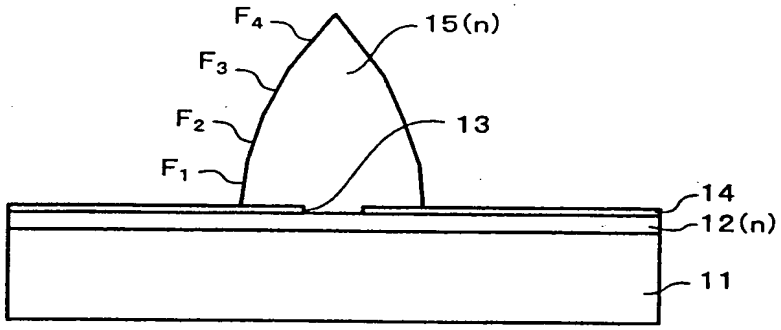

Fig. 4A

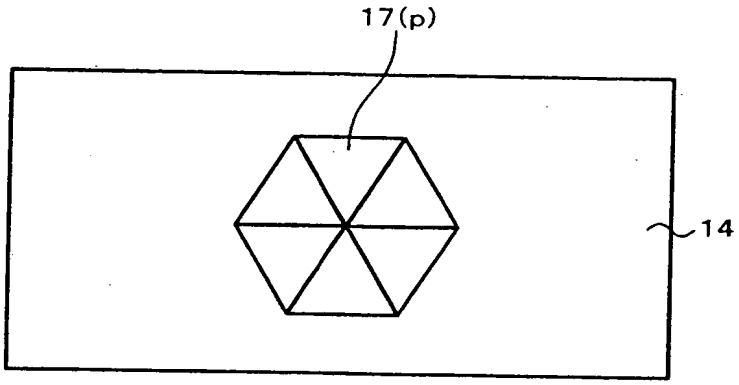

Fig. 4B

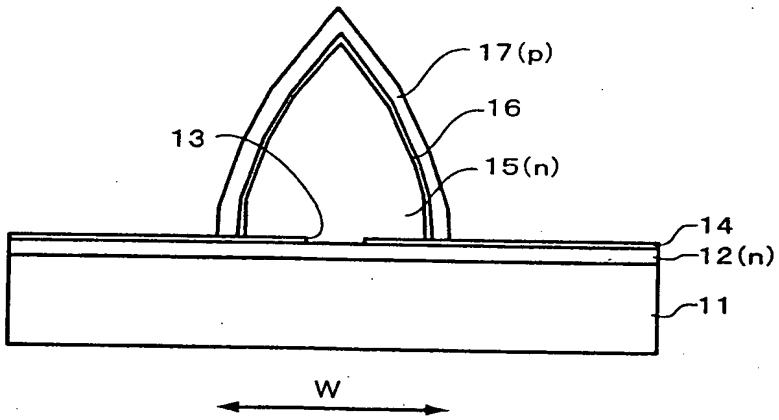

Fig. 5A

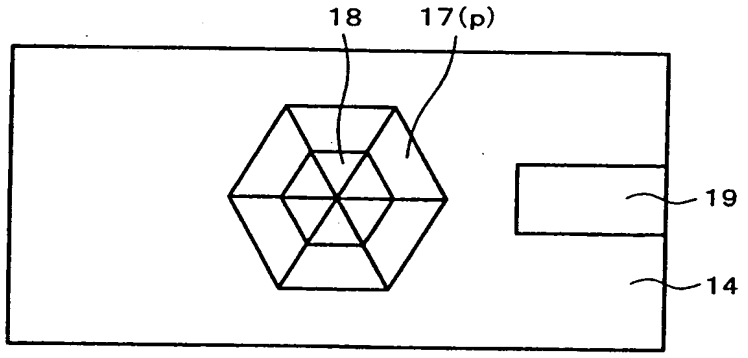

Fig. 5B

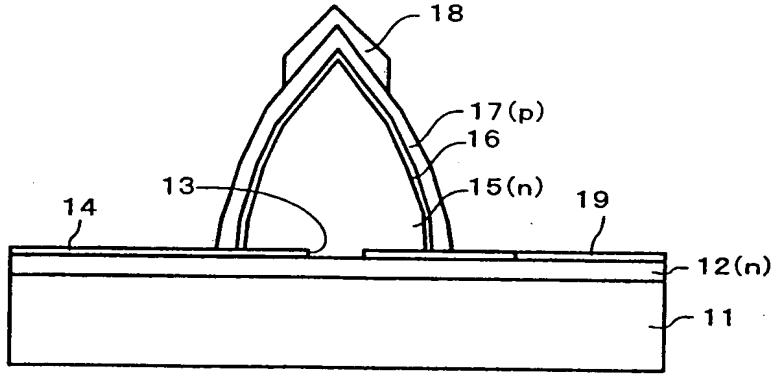

Fig. 6

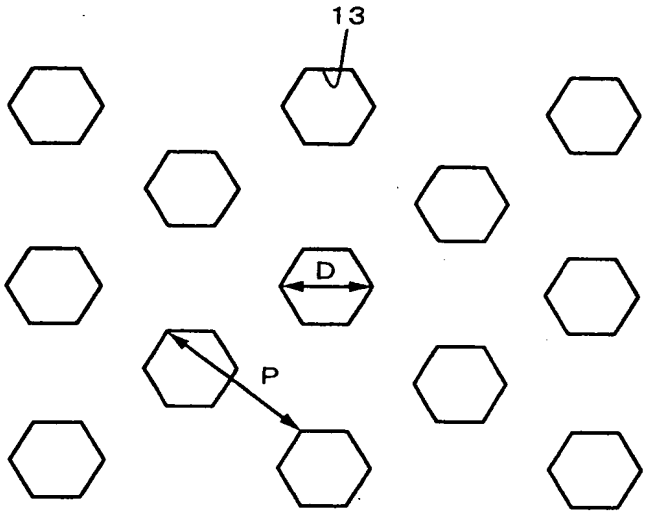

Fig. 7

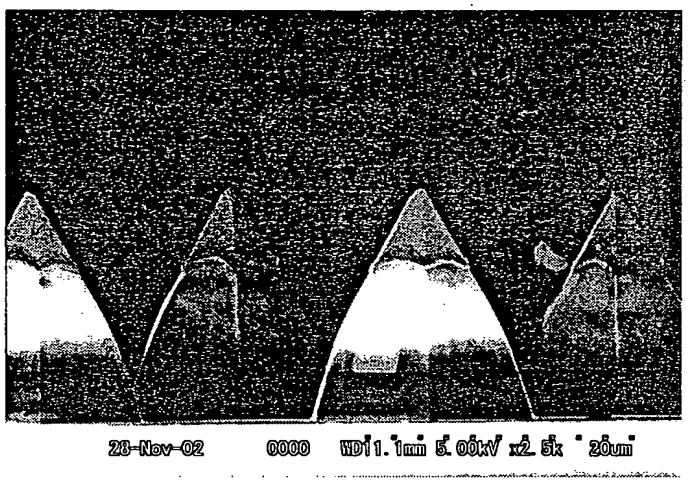
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Fig. 8

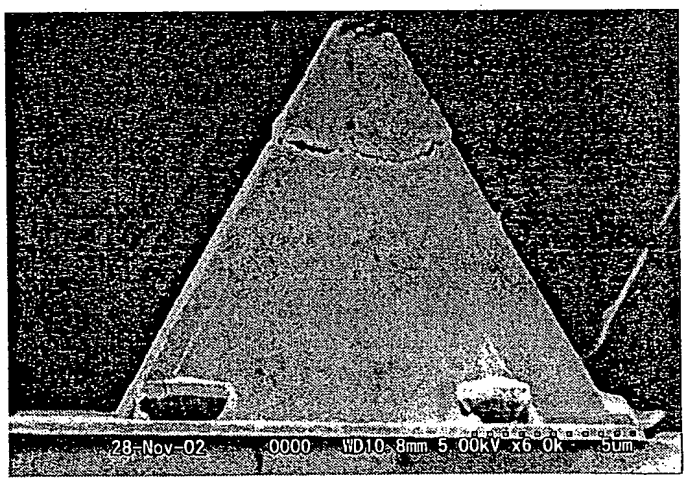
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Fig. 9

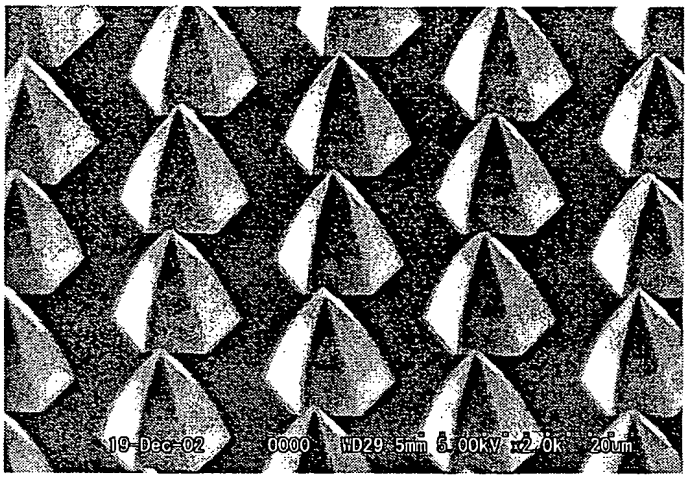

19-Dec-02 0000 WD29.5mm 5.00kV x2.0k 20um

Fig. 10

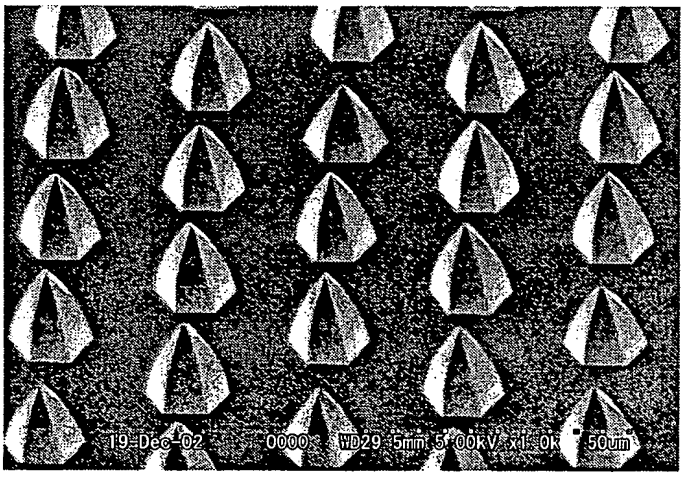

19-Dec-02 0000 WD29.5mm 5.00kV x1.0k 50um

Fig. 11

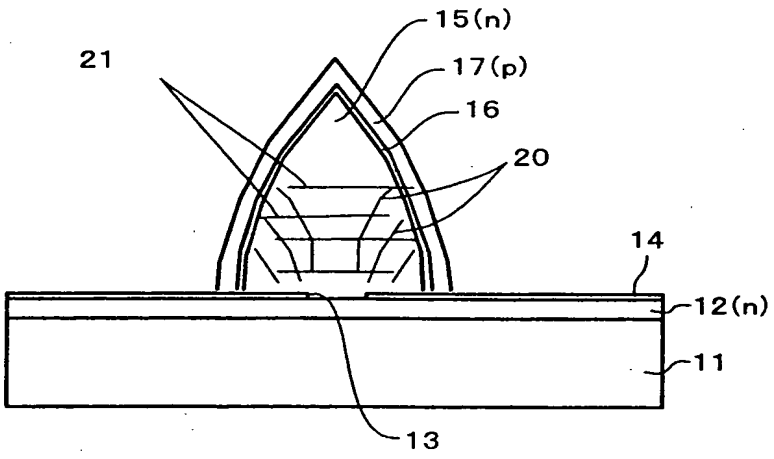


Fig. 12

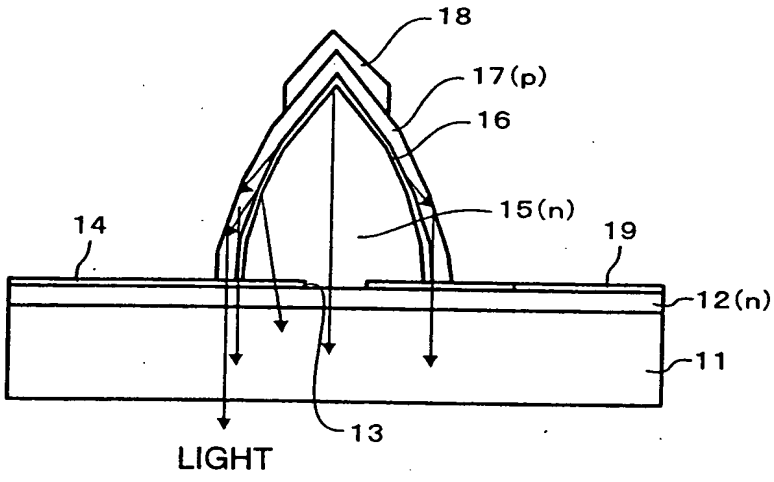


Fig. 13

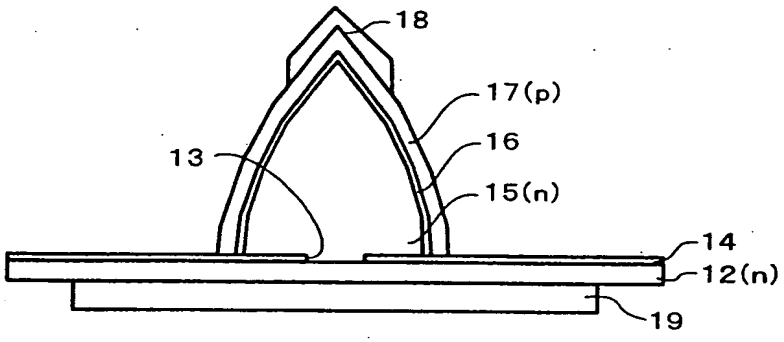


Fig. 14

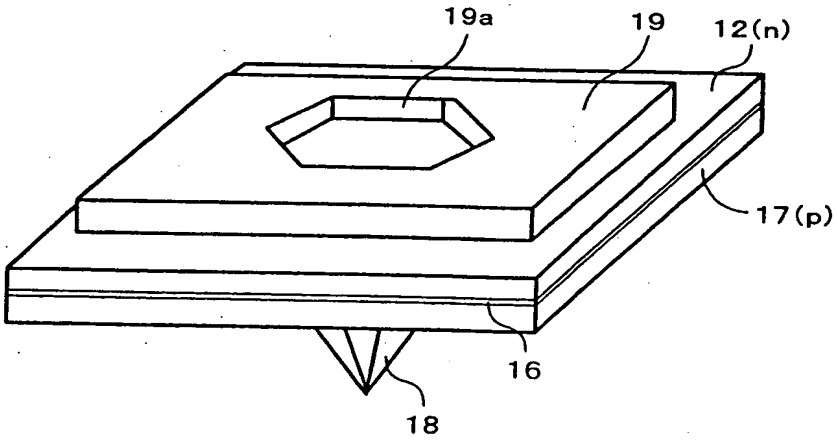


Fig. 15

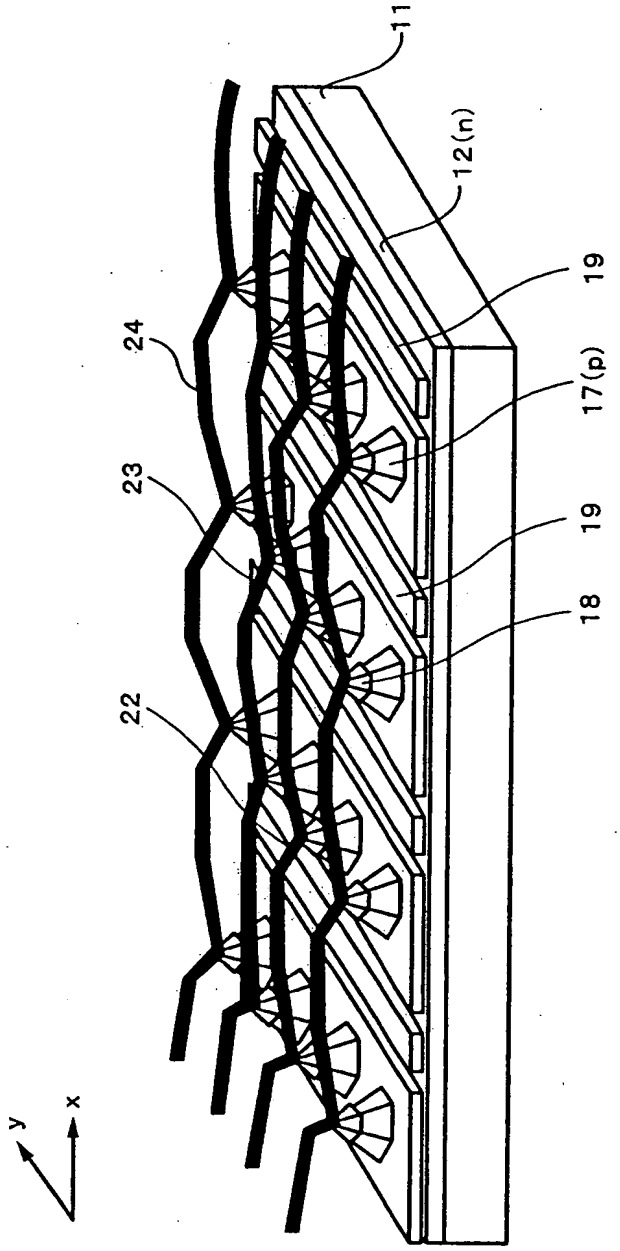


Fig. 16A

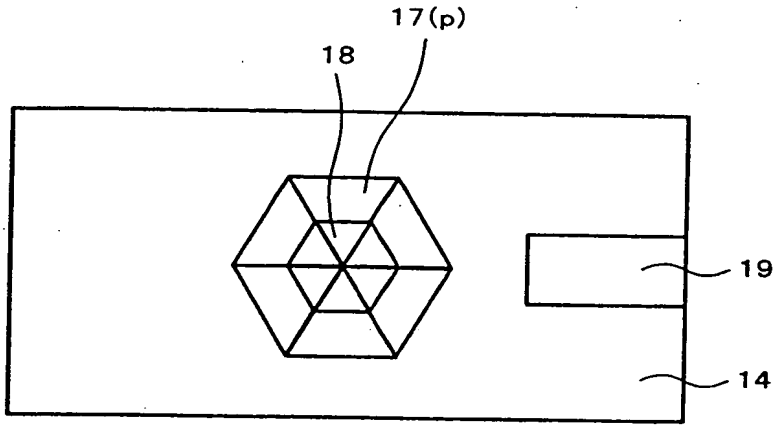


Fig. 16B

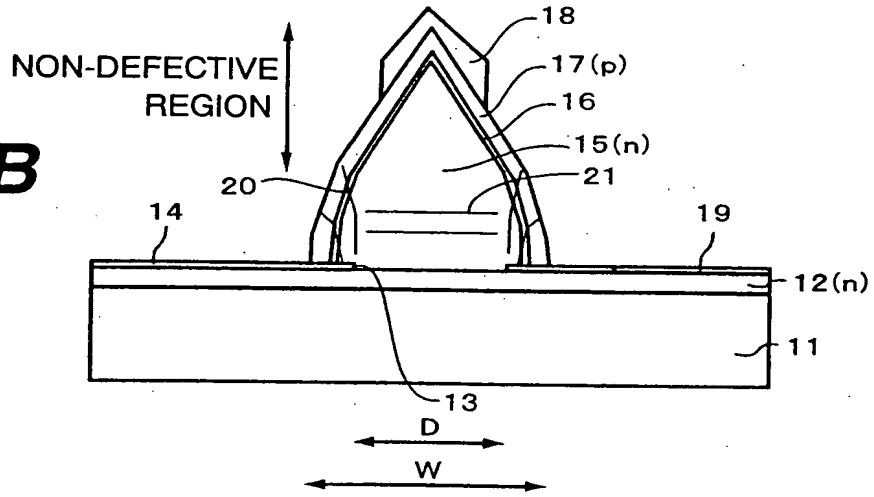


Fig. 17A

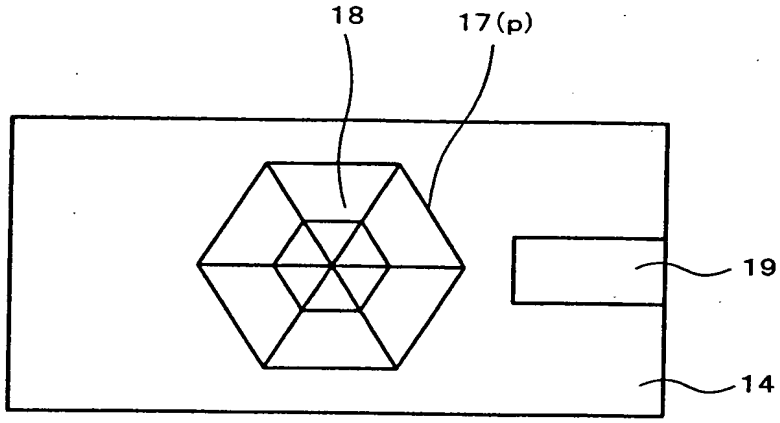


Fig. 17B

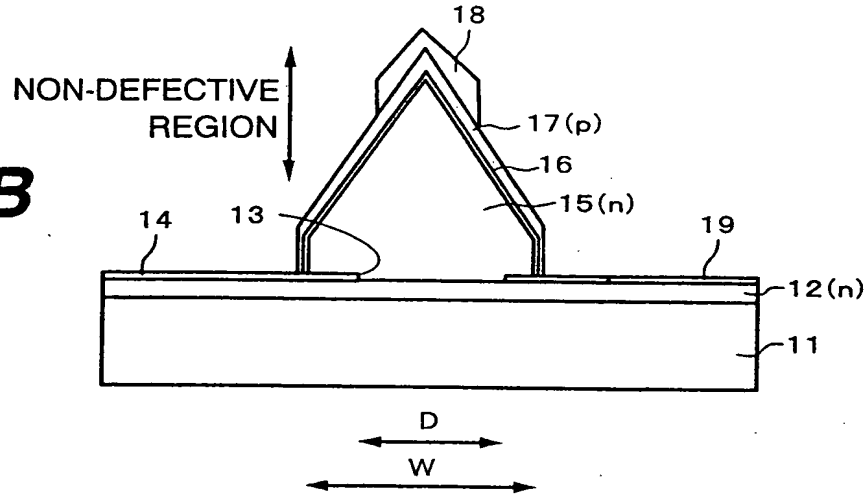


Fig. 18A

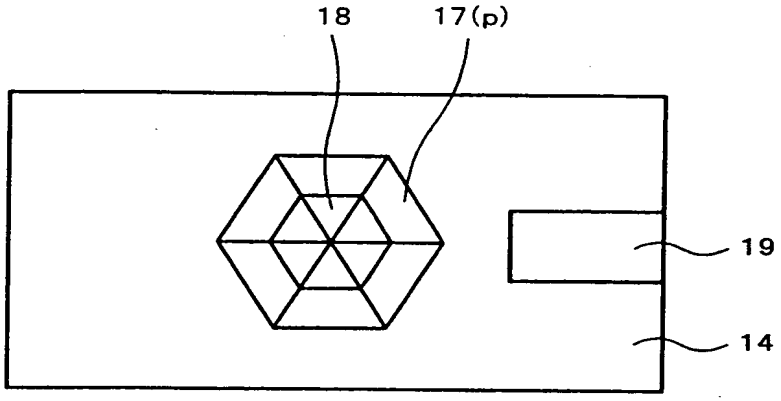


Fig. 18B

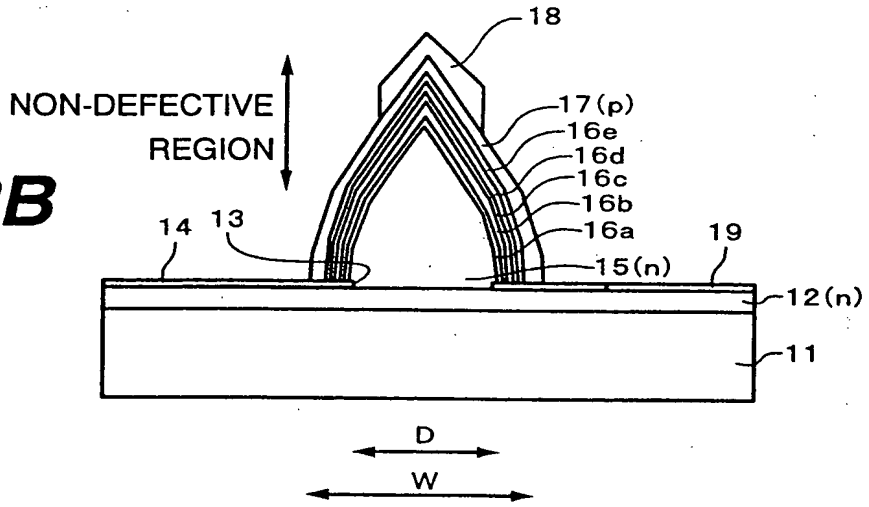


Fig. 19A

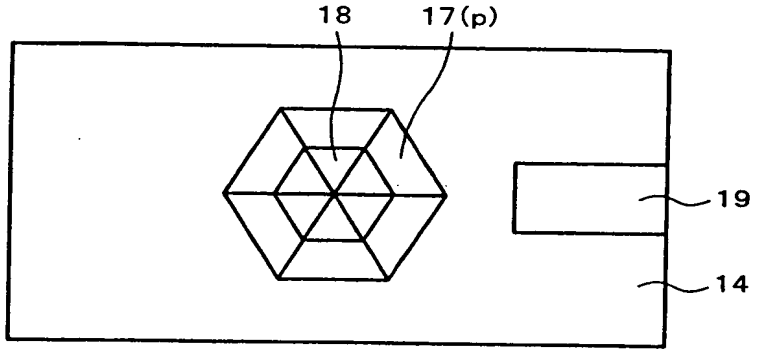


Fig. 19B

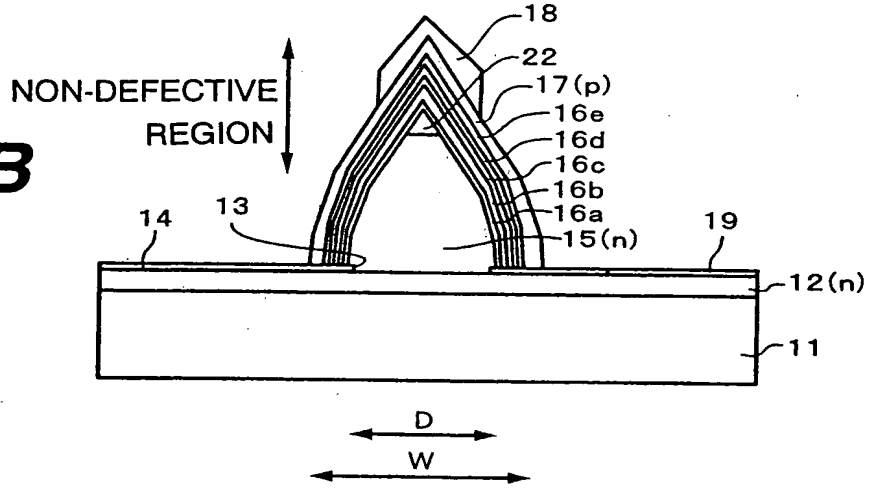


Fig. 20A

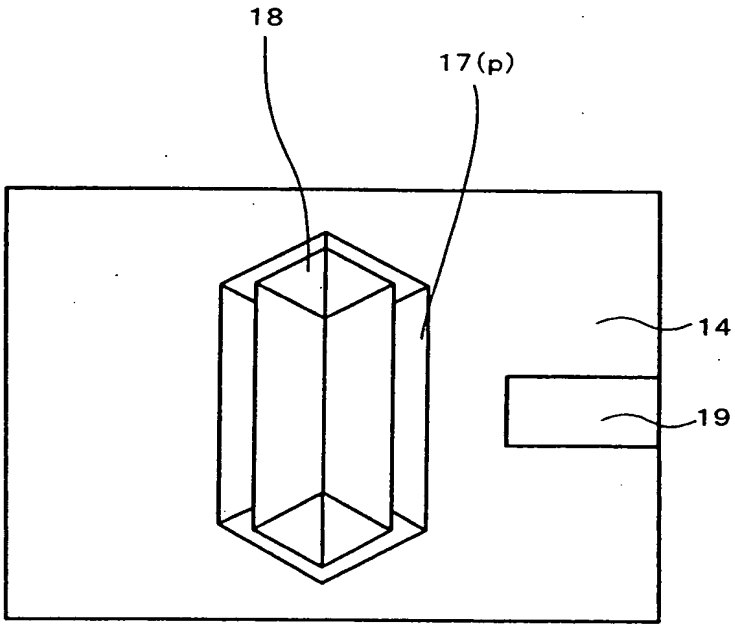


Fig. 20B

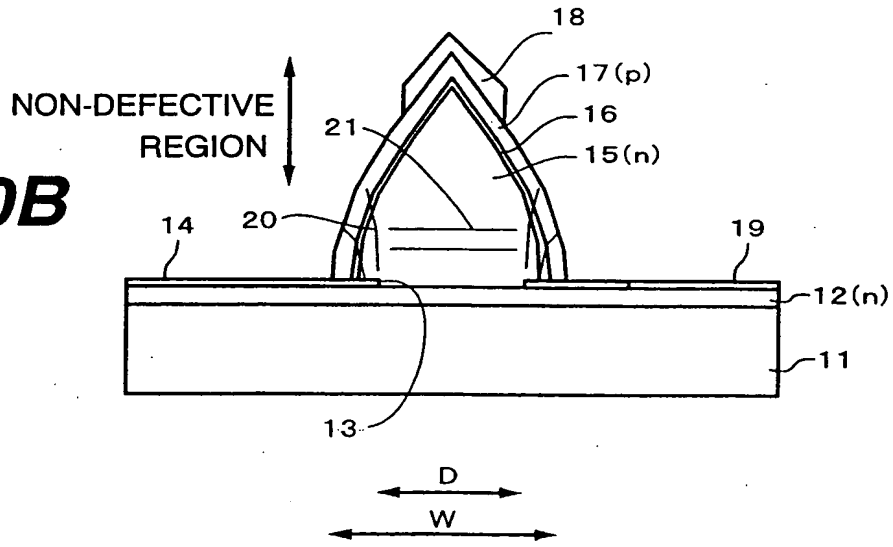


Fig. 21A

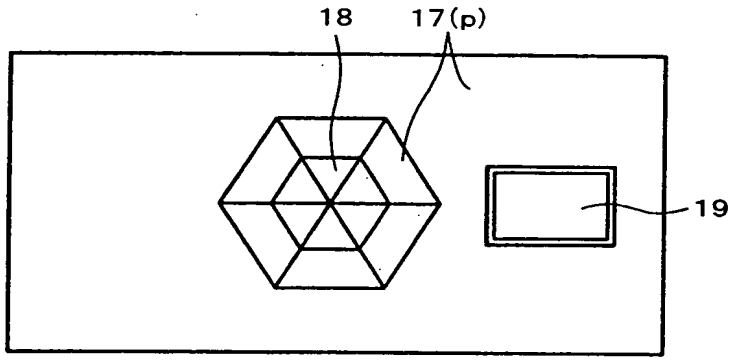
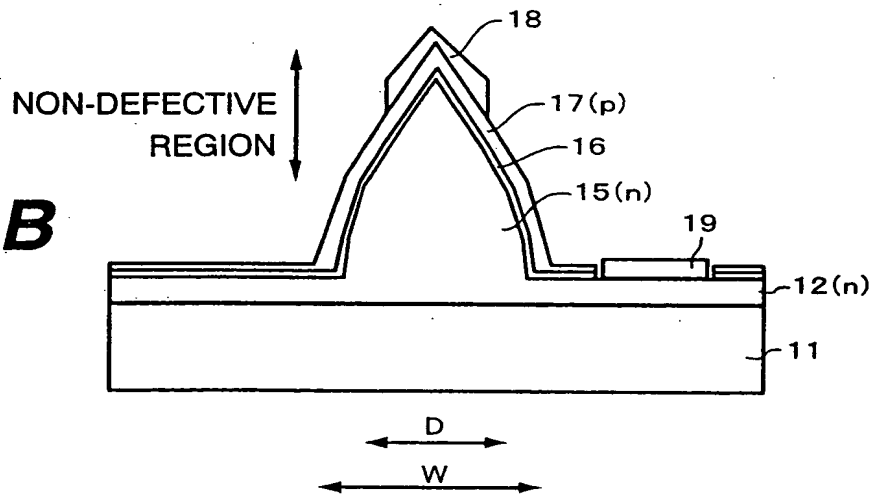


Fig. 21B



DESCRIPTION OF REFERENCE NUMERALS

11	SAPPHIRE SUBSTRATE
12	n-TYPE GaN LAYER
13	OPENING
14	GROWTH MASK
15	n-TYPE GaN LAYER
16	ACTIVE LAYER
17	p-TYPE GaN LAYER
18	p-SIDE ELECTRODE
19	n-SIDE ELECTRODE